memory device 123. The remaining memory modules 120 - 122 and 124 - 127 are supplied with a negative power source voltage (ground voltage) VSS via the respective dummy output enable terminal. Thus, only the memory device 123 is allowed to generate dummy output data, which will be described later. In the specification, clocks handled within the module are internal clocks.

Please replace page 10, paragraph 3, beginning at line 27, with:

The PLL circuit 16 receives dummy output data, which is output from the memory device 123 via the dummy output terminal P2. Then, the PLL circuit 16 compares the phase of the dummy output data with that of the external clock. As will be described later, the memory device 123 is capable of generating dummy output data from the clock received via the dummy data output terminal P2. The timing of the clock used to output data is adjusted by the PLL circuit 16 so that the dummy output data and the external clock are pulled in phase. If the dummy output data has the same delay amount as the data output signal lines 24, the dummy output data and the output data at the data input/output terminal DQ are in phase. That is, the output data at the data input/output terminal DQ is synchronized with the external clock. In that manner, the dummy output data functions as a phase adjustment signal.

IN THE CLAIMS:

Please cancel claim 28 without prejudice or disclaimer.

Please amend claims 1, 3, 17 and 25 as follows:

1. (Once Amended) A module comprising:

a semiconductor device;

a phase adjustment circuit which receives a phase adjustment signal output from said semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock; and

an output circuit that is provided in the semiconductor device and generates the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock.

3. (Once Amended) A module comprising:

semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal;

a phase adjustment circuit which receives the phase adjustment signal output from said first semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock, the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock.

17. (Once Amended) The module as claimed in claim 3, wherein:

the semiconductor devices including the first semiconductor device have an identical circuit configuration; and

a4 Cont

the output circuit of the first semiconductor device receives an external instruction that instructs the first semiconductor device to generate the phase adjustment signal.

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25. (Once Amended) A system comprising:

modules;

a wiring board on which the modules are mounted; and

a dummy output load line serving as loads of dummy output data output from the modules, wherein the modules comprise a module including:

semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal;

a phase adjustment circuit which receives the phase adjustment signal output from said first semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock, the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference from the phase adjustment signal and the first clock.

A copy of the marked up amended claims is attached to this response showing the changes as set forth in 37 C.F.R. § 1.121.